FILL THE VOID V - MITIGATION OF VOIDING FOR BOTTOM TERMINATED COMPONENTS

Tony Lentz
tlentz@fctassembly.com

Greg Smith
gsmith@blueringstencils.com

Originally presented at IPC APEX 2020.
Outline / Agenda

• Introduction
  • Voiding - Why all the Fuss?
  • Causes of Voiding

• Methodology

• Results and Discussion
  • Voiding by Stencil Thickness
  • Voiding by Area of Coverage
  • Voiding by Component
  • Voiding by I/O Pad Toe Adder

• Conclusions and Recommendations
Introduction
Voids - What is All the Fuss About?

- Mechanical Failure (Cracks)
- Overheating Failure
- Electric Signal Degradation (Noise)
- Hard to Rework!
Introduction
Voiding Causes

Print/Dispense
- Temp/Humidity
- Volume
- Storage Condition

Reflow
- Soak Temp
- Soak Time
- Peak Temp
- TAL
- BLT
- Ramp Rate
- Atmospheric Pressure
- Atmosphere

Void

Substrates / Components
- Solder Paste

- Storage Condition
- Surface Finish
- Mounting Alignment
- Oxidation Level
- Soldering area
- Surface Roughness
- Surface Tension of molten solder
- Flux Activity
- Powder Size/Oxidation Level
- Melting Temp Range
- Flux Vaporization Behavior
- Storage Condition
Introduction
Voiding Causes - What Can We Change?

- Easy to Change
  - Solder Paste
  - Stencil Design

- Harder to Change
  - Board Design & Components
  - Reflow Equipment (Vacuum)
  - Surface Finish
  - OSP
  - iSilver
  - ENIG
Methodology
**Methodology**

**Circuit Board and Stencil Design**

- QFN 10 mm, 7 mm, 4 mm
- FR4, 0.062”, 1 oz Cu, ENIG
- Thermal 70 & 60% Area of Coverage
- I/O Pad Toe Adder: 0, 5, 10, 20 mils
## Methodology

### Stencil Design Details

Two Stencil Thicknesses:
- 4 and 5 mil

<table>
<thead>
<tr>
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<td>4</td>
<td>20</td>
<td>133.5</td>
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## Methodology
### Reflow Profiles Tested

<table>
<thead>
<tr>
<th>Profile Name</th>
<th>Max Rise Slope (°C/sec)</th>
<th>Soak Time (150-200°C in sec)</th>
<th>Reflow Time (&gt;220°C in sec)</th>
<th>Peak Temp (°C)</th>
<th>Time (25°C-peak in min)</th>
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<tbody>
<tr>
<td>Linear ramp to spike</td>
<td>1.7-2.1</td>
<td>89-91</td>
<td>73-74</td>
<td>244-247</td>
<td>4.5-4.6</td>
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<tr>
<td>Short linear ramp</td>
<td>2.0-2.1</td>
<td>65-66</td>
<td>66-69</td>
<td>245-247</td>
<td>3.9</td>
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<tr>
<td>Short plus soak</td>
<td>2.0-2.1</td>
<td>92-94</td>
<td>52-55</td>
<td>242-245</td>
<td>4.3</td>
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<tr>
<td>Long linear ramp</td>
<td>1.6-1.8</td>
<td>87-89</td>
<td>94-97</td>
<td>249-251</td>
<td>5.4-5.5</td>
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<tr>
<td>Long plus soak</td>
<td>1.5-1.8</td>
<td>114-116</td>
<td>75-80</td>
<td>246-248</td>
<td>5.8-5.9</td>
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</tbody>
</table>
Methodology
Reflow Profile Chosen

- Linear Ramp to Spike (RTS)
- Lowest Voiding with the Solder Paste Used
Methodology

Statistics

Data sets shown as box plots & circles

95% confidence level

Connecting letters shows differences

<table>
<thead>
<tr>
<th>Level</th>
<th>Mean</th>
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<tr>
<td>70</td>
<td>11.2</td>
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<tr>
<td>60</td>
<td>9.5</td>
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</tbody>
</table>

Levels not connected by same letter are significantly different.
Methodology

Process

Print Solder Paste
Place & Reflow
Take Pictures
Measure Voiding

20 Boards Each 2 Stencils

Data

Inspection
Wetting / Solder Fillet
Bridging
Skew

Voiding
Void Area %
Largest Void %
Results
Results
I/O Solder Joints

QFN 10

No Bridging or Skew was Observed
Results
Voiding by Stencil Thickness

Overall

**60% Paste Area**

**70% Paste Area**
Results
Voiding by Area of Coverage

**4 mil Stencil**

**5 mil Stencil**
Results
Voiding by Component

Small QFN’s = Higher Voiding
Results
Voiding by Toe Adder

Increasing Length of Toe Adder = Lower Voiding
Results

Voiding by Toe Adder

Toe Adder Affects Voiding Regardless of Paste Area or Stencil Thickness
Results

Voiding Overall

High Voiding
Small QFN
4 mil Stencil
+0 to 5 Toe

Low Voiding
Large QFN
5 mil Stencil
+10 to 20 Toe
Conclusions and Recommendations
Conclusions

- The linear ramp to spike (RTS) profile produced the lowest voiding with the solder paste used.
- Increasing the stencil foil thickness from 4 mils to 5 mils reduced voiding significantly.
- Increasing area of coverage from 60 to 70% did not have a significant effect.
- Overall voiding decreases as QFN component body size is increased.
- Overprinting the I/O lead toes reduces void area, regardless of the other factors.
Recommendations to Mitigate Voiding

✓ Use a low voiding solder paste with the appropriate reflow profile.
✓ Increase stencil thickness or area of coverage on thermal pads.
✓ Overprint to the toe of the QFN I/O pads.