FILL THE VOID IV: ELIMINATION OF INTER-VIA VOIDING

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OUTLINE

- Introduction
- Factors that Influence Voiding
- Methodology
- Voiding Results
- Recommendations to Fill the Void
- Future Work
- Acknowledgements
- Thank You & Questions
INTRODUCTION
VOIDING

Voiding is Common for QFN Thermal Pads with Via Holes
FACTORS THAT INFLUENCE VOIDING FOR VIA-IN-PAD DESIGNS

Via Hole Plugging Options: Open, S/M Tent, Plugged
FACTORS THAT INFLUENCE VOIDING FOR VIA-IN-PAD DESIGNS

Solder Paste Print Options: Print over Vias, Print around Vias
METHODOLOGY
PR Test Board with Via in Pad (0.3 mm = 12 mil vias), Plated with ENIG
PR Test Board with a Solder Mask Tent on the Bottom Side
PR Test Board with Non-Conductive Via Fill, Plated with Cu and ENIG
QFN Components: 10 mm body (68 lead) and 7 mm body (48 lead). Matte Tin Finish
Standard Solder Paste Print: 65% Area Window Pane. Printed Over Via Holes
METHODOLOGY – MODIFIED STENCIL

Modified Solder Paste Print: 63% Area Grid. Printed Around Via Holes
No Clean SAC305 Type 3 Solder Paste

METHODOLOGY – SOLDER PASTE AND REFLOW

<table>
<thead>
<tr>
<th>Setting</th>
<th>RTS Profile</th>
</tr>
</thead>
<tbody>
<tr>
<td>Ramp rate</td>
<td>1.7 – 1.8 °C/sec</td>
</tr>
<tr>
<td>Reflow Time (&gt; 220 °C)</td>
<td>61 – 67 sec</td>
</tr>
<tr>
<td>Peak temperature</td>
<td>241 to 248 °C</td>
</tr>
<tr>
<td>Profile length (25 °C to peak)</td>
<td>4.70 minutes</td>
</tr>
</tbody>
</table>
METHODOLOGY – EXPERIMENTAL PROCEDURE

- 10 Circuit Boards For Each Variation
- 4 of Each QFN Size Placed and Boards were Reflowed
- Void Area and Largest Size Measured on Each QFN
- Images were Taken of Representative QFN Voiding
- Data was Analyzed and Statistics Generated
VOIDING RESULTS
## VOIDING RESULTS – VIA FILL OPTIONS, STANDARD STENCIL

<table>
<thead>
<tr>
<th></th>
<th>Open Vias (No Fill)</th>
<th>Solder Mask Tent</th>
<th>Complete Plug</th>
<th>Flat Thermal Pad (No Via)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>QFN7</strong></td>
<td><img src="image1" alt="Image" /></td>
<td><img src="image2" alt="Image" /></td>
<td><img src="image3" alt="Image" /></td>
<td><img src="image4" alt="Image" /></td>
</tr>
<tr>
<td><strong>QFN10</strong></td>
<td><img src="image5" alt="Image" /></td>
<td><img src="image6" alt="Image" /></td>
<td><img src="image7" alt="Image" /></td>
<td><img src="image8" alt="Image" /></td>
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3D Voiding Images: Open Vias = Lower Voiding, Plugged and No Vias = More Voiding
VOIDING RESULTS – VIA FILL OPTIONS, MODIFIED STENCIL

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<tr>
<td><strong>QFN10</strong></td>
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<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
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3D Voiding Images: Open Vias = Lower Voiding, Plugged Vias = More Voiding
VOIDING SIZE – BY STENCIL

PR = Flat Pad (No Vias)
PR Plug = Plugged Vias
PR Tent = S/M Tented Vias
PR Via = Open Vias

STANDARD STENCIL

MODIFIED STENCIL
SOLDER FLOW TO THE BOTTOM OF THE BOARD

STANDARD STENCIL

MODIFIED STENCIL
VOIDING SIZE BY STENCIL DESIGN FOR EACH VIA TYPE

**OPEN VIAS**

**TENTED VIAS**

**PLUGGED VIAS**
VOIDING BY QFN SIZE

LARGEST VOID SIZE

VOID AREA

Standard Stencil (65%)
Flat QFN Pads – No Vias
QFN10 Mass = 2x QFN7
FILL THE VOID
RECOMMENDATIONS TO FILL THE VOID

- Void size can be reduced using via holes in QFN thermal pads.
- Modifications to the stencil design limits the amount of solder flow through the via holes.
- Use of larger QFN's may reduce overall voiding.
FUTURE WORK

Work on mitigation strategies to reduce voiding is ongoing. Data will be presented at future technical conferences.
ACKNOWLEDGEMENTS

Greg Smith with BlueRing Stencils designed and supplied the stencils used in this work.
Thank You!

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