

FILL THE VOID III

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ABSTRACT

This study is part three in a series of papers on voiding in solder joints and methods for mitigation of voids. In this study several new variables were tested and compared to previous data on voiding. A new circuit board design was used which is different than the circuit board used in previous studies. The new circuit board design includes two sizes of QFNs (Quad Flat No Lead), BGA's (Ball Grid Array), and LGA (Land Grid Array) components which are susceptible to voiding.

The following variables were evaluated with respect to voiding:

- Solder powder size was varied using a no-clean lead-free solder paste and IPC Type 3, Type 4 and Type 5 SAC305 solder powders.
- Solder alloy was studied using SAC305 alloy, SN100C® alloy, SN100CV® alloy and a mixture of SAC305/SN100C alloys.
- Surface finish on the circuit board is thought to have an impact on voiding. OSP surface finish is more difficult to wet with solder than other surface finishes and in theory should produce higher voiding levels, and this was evaluated with multiple solder pastes.
- The performance of a new “low voiding” no clean solder paste was compared to other industry standard no clean solder pastes.
- Several new stencil designs on QFN thermal pads were tested.

These voiding results were summarized along with previous data on voiding and recommendations given to help the reader “Fill the Void.”

Key words: voids, solder joint, solder paste, solder powder size, solder alloy, surface finish, stencil design, QFN

INTRODUCTION

Voids are gaps in a solder joint where the solder does not completely fill the space between the component and circuit board (Figure 1).

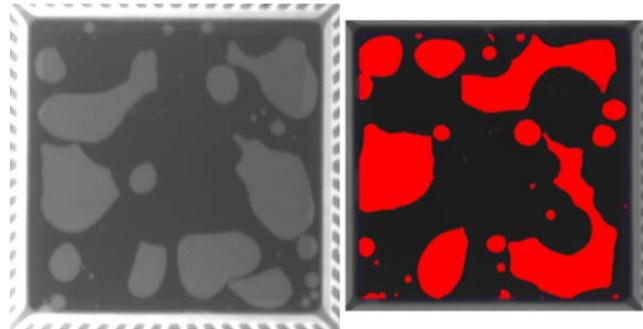


Figure 1: Voiding in QFN thermal pad solder joints

Voids can be caused by a variety of things. Often voids are created by the interaction between multiple factors (Figure 2).

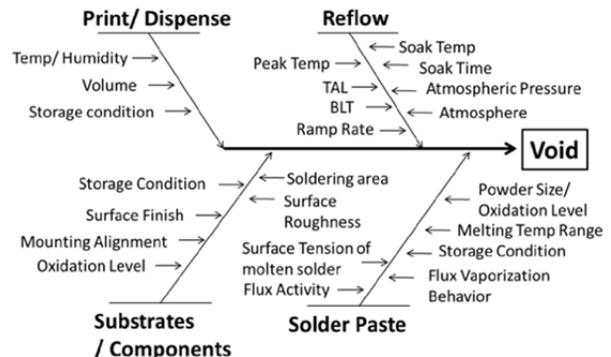


Figure 2: Factors That Influence Voiding [1]

Many of these factors were tested in previous work [2, 3]:

- A variety of solder pastes were evaluated for voiding potential.
- Solder powder size and manufacturer were varied.
- Stencil design on QFN thermal pads was modified.
- The surface finish on the circuit boards (ENIG and OSP) was varied.
- Multiple reflow profiles in the convection oven were used.
- Nitrogen was evaluated in convection reflow.
- Vapor phase reflow was used with and without vacuum.

All of these factors were compared and contrasted with respect to voiding.

This investigation continues with previous work and expands upon the factors that were tested. Solder powder size was originally tested with one solder paste flux and the voiding levels were shown to decrease with decreasing

particle size. This work was repeated with a different solder paste to determine if the voiding reduction applies to multiple solder pastes. In previous work SAC305 was the only solder alloy tested. In this work, SN100C alloy, SN100CV alloy, and a mixture of SAC305 and SN100C (AT mixture) were evaluated for voiding performance. The voiding impact of electroless nickel immersion gold (ENIG) versus organic solderability preservative (OSP) surface finish was expanded to include additional solder pastes. A new “low voiding” no clean solder paste was evaluated for voiding performance and compared to industry standard solder pastes. Lastly, stencil design was further investigated with respect to voiding on QFN thermal pads. Voiding over an 8 hour stencil life was not able to be included in this work, but it will be planned for future studies.

EXPERIMENTAL METHODOLOGY

This experiment uses a test circuit board called Print and Reflow Test Board (PR Test Board - Figure 3). This circuit board is made of FR4 material with etched copper pads that have an ENIG surface finish. OSP surface finish was also used in some tests for comparison to ENIG.

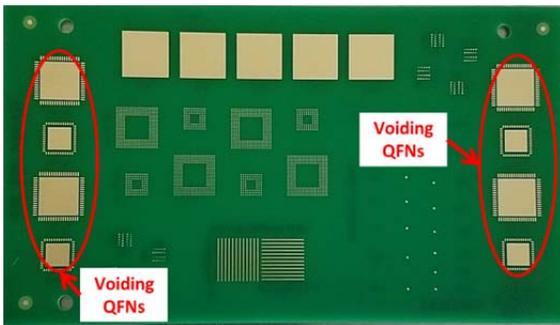


Figure 3: PR Test Board Voiding Areas

This PR test board has four 10mm QFN68 and four 7mm QFN48 components. The components used were “dummy” components with a matte tin finish. Voiding was measured on the QFN thermal pads.

The solder pastes used in this study were chosen for their voiding potential. Water soluble lead free solder paste B has relatively high voiding potential and was used for most of the experiments. The intention of using solder paste B was to increase the scale of measurement in order to compare and contrast the factors that contribute to voiding. No clean lead free solder paste C was chosen because it has low voiding potential. Solder paste C was used as a low voiding comparison to solder paste B in some experiments. No clean lead free solder paste F is a new product that was formulated with “ultra-low” voiding potential. Solder paste F was compared to solder paste C in some experiments in order to demonstrate the lowest possible voiding.

Solder alloy was varied in this study in order to determine the effects of alloy on voiding. The alloys used are listed in Table 1 below.

Table 1: Solder Alloys Studied for Voiding Potential

Alloy	Composition (% wt)	Melting Range (°C)
SAC305	Sn / 3.0 Ag / 0.5 Cu	217 - 220
SN100C	Sn / 0.7 Cu / 0.06 Ni / 0.005 Ge	227 (eutectic)
SN100CV	Sn / 1.5 Bi / 0.7 Cu / 0.06 Ni	221 - 225
SAC305 90% SN100C 10%	Sn / 2.7 Ag / 0.52 Cu / 0.006 Ni	217 - 227

These solder alloys were chosen due to the differences in their melting ranges. In theory, wider melting ranges allow for slower freezing behavior which gives more time for gas bubbles to escape the solder joints. This theory was evaluated through voiding measurements.

Two different stencil designs were used for the QFN thermal pads. The stencils were made of 127 micron (5 mils) thick fine grain stainless steel. No nano-coatings were used. The first stencil design used a standard nine window pane cross hatch on each QFN location (Figure 4).

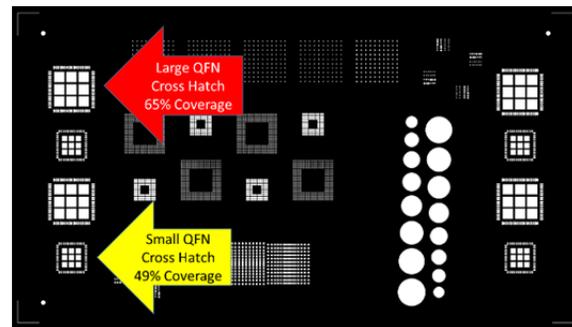


Figure 4: First Stencil Design with Standard Cross Hatch on QFN Thermal Pads

The circuit board design for the QFN thermal pads is as follows. The large QFN thermal pad is 8.30 mm (327 mils) square. The small QFN thermal pad is 4.90 mm (193 mils) square. The stencil design for the QFN thermal pads is as follows. The large QFN cross hatch pattern has nine 2.24 mm (88 mil) square windows and a 0.51 mm (20 mil) wide web for a net of 65% area coverage. The small QFN cross hatch pattern has nine 1.15 mm (45 mil) square windows and a 0.38 mm (15 mil) wide web for a net of 50% area coverage.

The second stencil has different cross hatch designs at each QFN location (Figure 5).

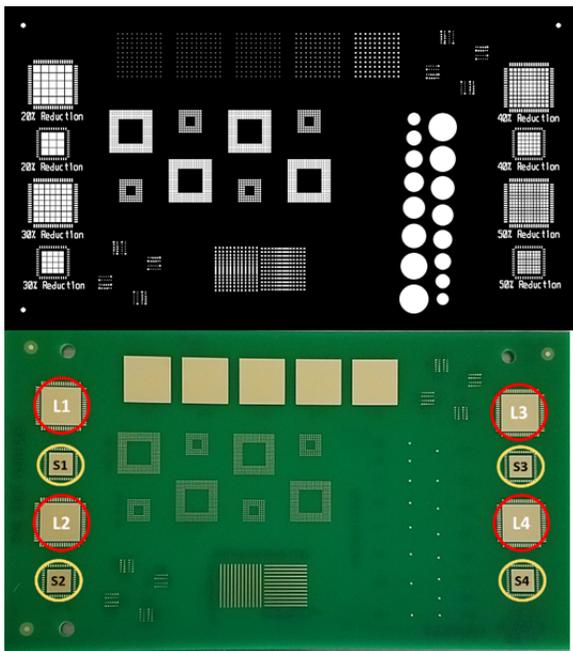


Figure 5: Second Stencil Design by QFN Location

The second stencil design details for each QFN location are shown in Table 2.

Table 2: Second Stencil Design for Voiding

Location	Number of Windows	Window Size in mm (mils)	Web Spacing in mm (mils)	Paste Coverage Area (%)
L1	25	1.47 (58)	0.20 (8)	80
L2	49	1.00 (39)	0.20 (8)	70
L3	100	0.64 (25)	0.20 (8)	60
L4	169	0.44 (17.5)	0.20 (8)	50
S1	9	1.47 (58)	0.20 (8)	80
S2	16	1.02 (40)	0.20 (8)	70
S3	36	0.64 (25)	0.20 (8)	60
S4	64	0.43 (17)	0.20 (8)	50

The number of windows and size of windows was varied at each location in order to generate a certain area of solder paste coverage. The solder paste coverage area was varied at 80, 70, 60, and 50% for both the large (10 mm) and small (7 mm) QFNs.

Two different reflow profiles were used and these were specific to the solder alloys. The SAC305 and SAC305 90% / SN100C 10% solder pastes were run through the SAC305 profile. The SN100C and SN100CV solder pastes were run through the SN100C profile. Both profiles were set up in a 10 zone convection reflow oven and are standard ramp to spike (RTS) linear profiles (Figure 6).

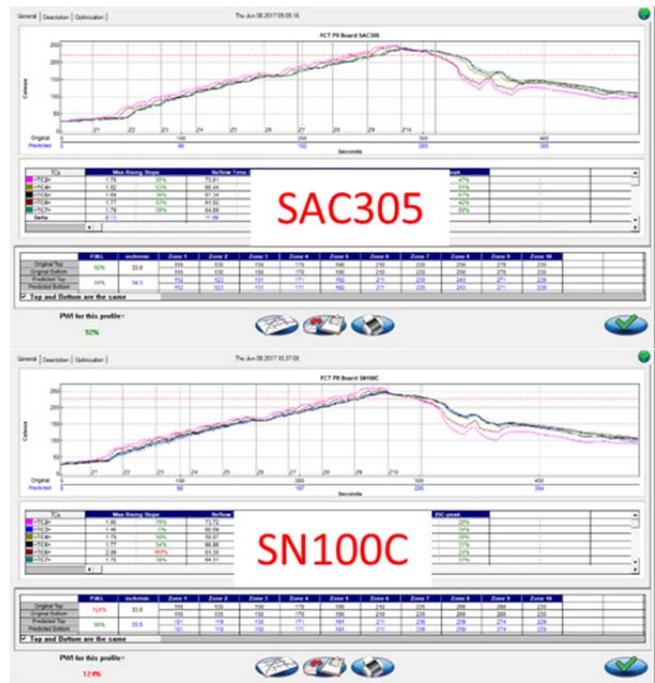


Figure 6: Ramp To Spike Profiles (Top = SAC305, Bottom = SN100C)

The SAC305 profile has a peak temperature of 241 to 248 °C. The SN100C profile has a higher peak temperature of 245 to 256 °C. A summary of the reflow profile parameters is shown below (Table 3).

Table 3: Reflow Profile Summary

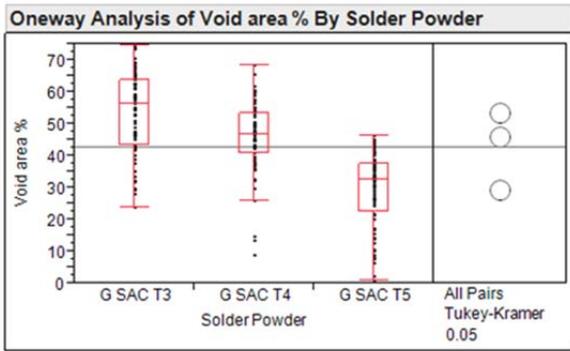
Setting	SAC305 Profile	SN100C Profile
Ramp rate	1.7 – 1.8 °C/sec	1.5 – 2.0 °C/sec
TAL (Reflow time)	61 – 67 sec > 221°C	60 – 67 sec > 227°C
Peak temperature	241 to 248 °C	245 to 256 °C
Profile length (25 °C to peak)	4.7 minutes	4.5 minutes

The X-ray system used to measure voiding was a 2D system that analyzes gray-scale to calculate voiding area. The X-ray source was set to a voltage of 70 kV and a current of 400 µA.

RESULTS

Solder Powder Size Effects on Voiding

In previous work [3] voiding by solder powder size was measured using water soluble solder paste B and SAC305 Type 3, Type 4 and Type 5 solder powders (Figure 7). This work was expanded with no clean solder paste C and “low voiding” no clean solder paste F (Figures 8 and 9).



Excluded Rows 1616

Means Comparisons

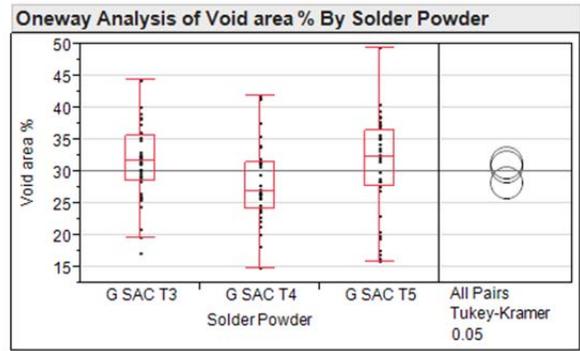
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
G SAC T3 A	53.348750
G SAC T4 B	46.000000
G SAC T5 C	29.266250

Levels not connected by same letter are significantly different.

Figure 7: Voiding by SAC305 Solder Powder Size for Solder Paste B



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Means Comparisons

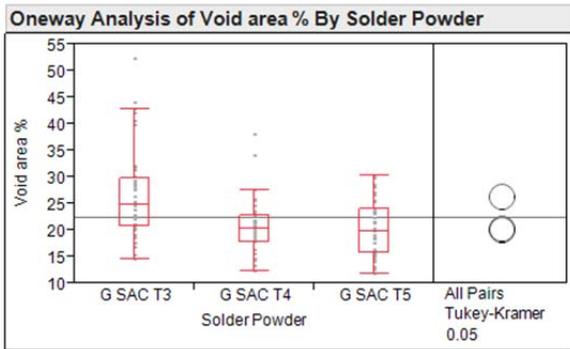
Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
G SAC T3 A	31.560000
G SAC T5 A	30.732500
G SAC T4 A	28.230000

Levels not connected by same letter are significantly different.

Figure 9: Voiding by SAC305 Solder Powder Size for Solder Paste F



Excluded Rows 120

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
G SAC T3 A	26.532500
G SAC T4 B	20.552500
G SAC T5 B	20.210000

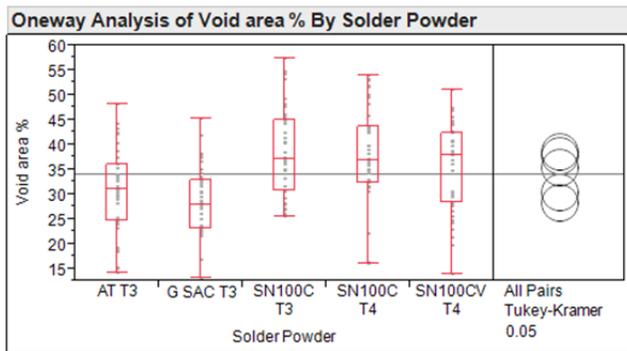
Levels not connected by same letter are significantly different.

Figure 8: Voiding by SAC 305 Solder Powder Size for Solder Paste C

Solder paste B showed decreasing void area as solder powder size decreased (T3 > T4 > T5). Solder paste C also showed a decrease in void area from Type 3 to Type 4 and Type 5 solder powders. Type 4 and Type 5 solder powders showed similar voiding with solder paste C (T3 > T4 = T5). Solder paste F did not show the same trend. The void levels were similar for all three solder powder sizes for solder paste F (T3 = T4 = T5). It is clear from these results that solder powder size does affect voiding for some solder pastes, but not all solder pastes. This is similar to voiding results found by Nash, and Lasky [4].

Solder Alloy Effects on Voiding

Four solder powder alloys were studied for their effects on voiding: SAC305 Type 3, SN100C Types 3 and 4, SN100CV Type 4, and SAC305 90% / SN100C 10% (AT mixture, Type 3). Solder paste B was used as the test vehicle for these alloys and the results are shown below (Figure 10).



Excluded Rows 520

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
SN100C T3 A	38.512500
SN100C T4 A	37.955000
SN100CV T4 A B	35.382500
AT T3 B C	30.500000
G SAC T3 C	28.440000

Levels not connected by same letter are significantly different.

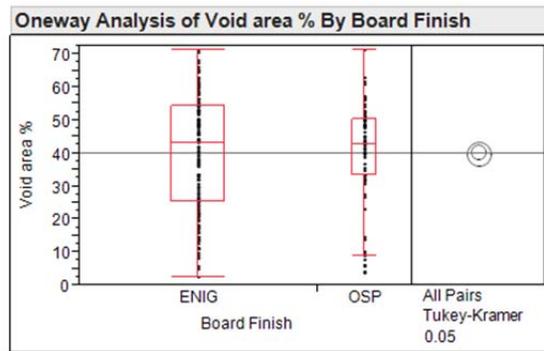
Figure 10: Voiding by Solder Alloy for Solder Paste B

The highest voiding was generated by SN100C Type 3 and 4 solder powders. SN100CV alloy gave statistically similar voiding to SN100C and the AT mixture (SAC305 90% / SN100C 10%). The AT mixture gave lower voiding than SN100C but similar voiding to SN100CV and SAC305. SAC305 gave lower overall voiding than SN100C and SN100CV.

The trend in voiding roughly follows the width of the melting range of the alloys. SN100C melts at one temperature and gave the highest voiding. SN100CV has a 4 degree C melting range and gave moderate voiding. SAC305 has a 3 degree C melting range and gave low voiding. The AT mixture has a melting range of 10 degrees C and gave low voiding. As the melting range widened, voiding tended to decrease.

Surface Finish Effects on Voiding

Voiding was studied in previous work [3] with both ENIG and OSP surface finishes and solder paste B (Figure 11).



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Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

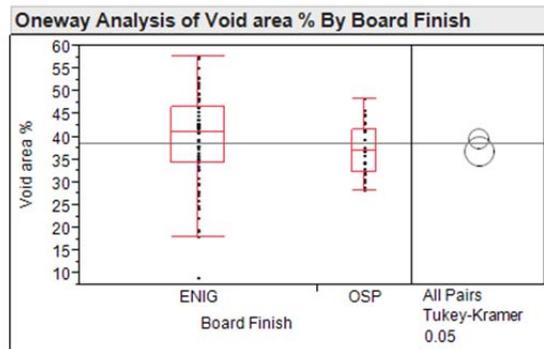
Connecting Letters Report

Level	Mean
ENIG A	40.151500
OSP A	40.056250

Levels not connected by same letter are significantly different.

Figure 11: Voiding by Surface Finish for Solder Paste B

Voiding for ENIG and OSP surface finishes was very similar with solder paste B. This test was repeated with another water soluble solder paste E (Figure 12).



Excluded Rows 1744

Means Comparisons

Comparisons for all pairs using Tukey-Kramer HSD

Connecting Letters Report

Level	Mean
ENIG A	39.597500
OSP A	36.943750

Levels not connected by same letter are significantly different.

Figure 12: Voiding by Surface Finish for Solder Paste E

Again voiding levels were similar for both ENIG and OSP surface finishes with solder paste E. The same is not true for no clean solder paste C (Figure 13).

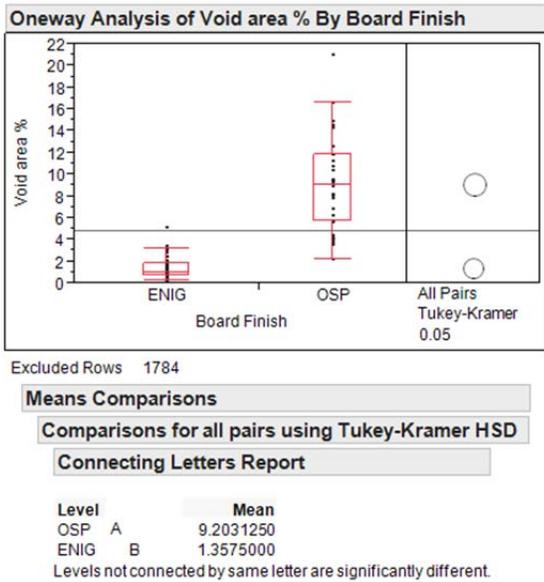


Figure 13: Voiding by Surface Finish for Solder Paste C

Voiding was significantly lower for ENIG surface finish than OSP surface finish with no clean solder paste C. This result shows that surface finish can affect voiding levels for certain solder pastes.

Solder Paste Effects on Voiding

It has become common for solder paste manufacturers to formulate solder pastes with the specific intention of reducing voiding [5]. A newly released “ultra-low voiding” solder paste F was compared to an industry standard solder paste C for voiding performance (Figure 14).

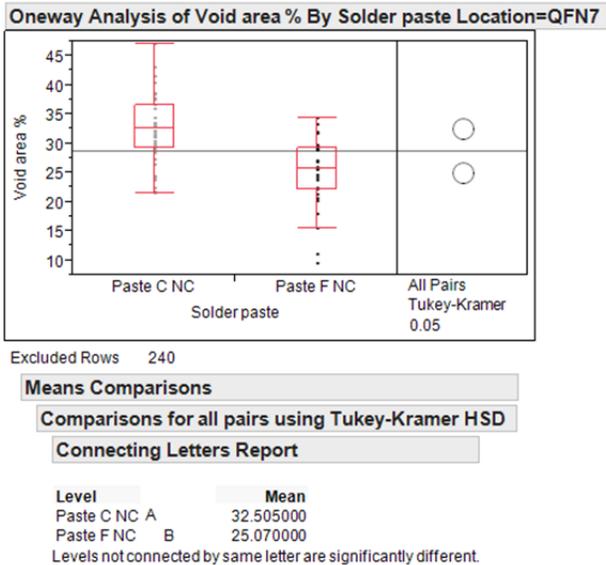


Figure 14: Voiding Comparison of Solder Pastes C and F

Solder paste F generated significantly lower voiding than solder paste C in this experiment. Solder paste is certainly a major factor amongst the potential factors which influence voiding [6]. Use of a lower voiding solder paste can reduce the overall potential for voiding.

Stencil Design Effects on Voiding

In prior work stencil design was varied [2] and voiding was studied for solder paste B (Figure 15). One particular stencil design (U11) was found to generate higher voiding than three other designs.

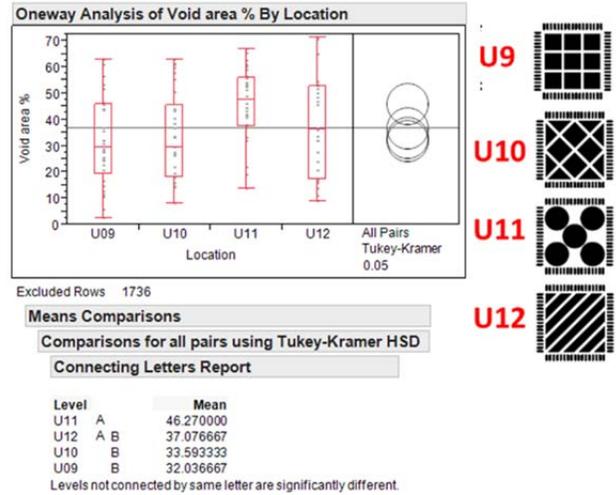


Figure 15: Voiding by Stencil Design for Solder Paste B

In this work four different stencil designs were tested (Figure 5) along with solder paste F. The area of solder paste coverage was varied from 50 to 80% on the QFN thermal pads. The voiding results are shown below (Figure 16).

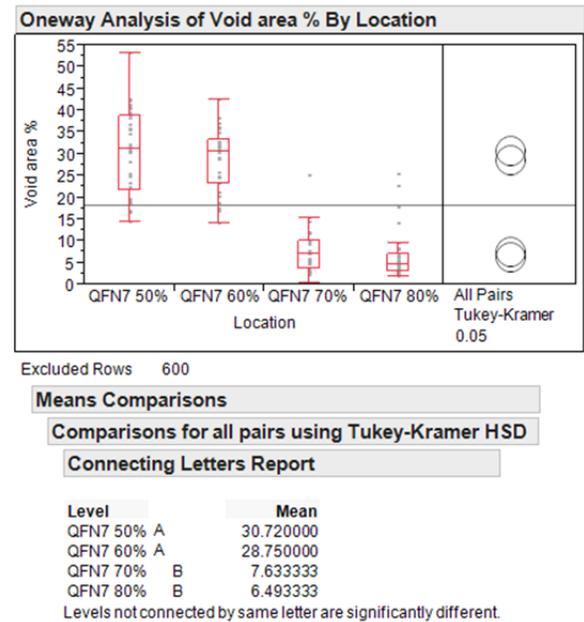


Figure 16: Voiding by Stencil Design for Solder Paste F

It is clear that 50 and 60% solder paste coverage generates much higher voiding than 70 and 80% coverage. It is worth noting that some component float and skew was seen for the 70 and 80% coverage areas. It is possible that the solder

paste could not fully wet the component and circuit board pads when the solder paste coverage became too low. Incomplete wetting is known to lead to void formation. [7].

CONCLUSIONS

What have we learned about voiding?

- Solder powder particle size affects voiding for some solder pastes. Voiding tends to decrease as solder powder size becomes smaller.
- Solder alloy affects voiding and seems to follow a trend with melting range. Wider melting ranges tend to generate lower voiding levels. Voiding could be influenced by other factors related to the solder alloys which were not evaluated in this study.
- OSP surface finish gave higher voiding than ENIG surface finish for a no clean lead free solder paste that was tested. Two different water soluble lead free solder pastes showed similar voiding levels for OSP and ENIG finishes.
- New “low voiding” solder pastes are becoming more common in our industry. In this work, low voiding solder paste F showed lower voiding than an industry standard solder paste C.
- Stencil design has an impact on voiding. In this study, area of printed solder paste coverage was varied. Voiding levels were much higher for 50 to 60% solder paste coverage than for 70 to 80% solder paste coverage.

Based on the results of this work, here are recommendations to help “Fill the Void.”

1. Use of smaller solder powder sizes can reduce voiding with certain types of solder paste.
2. Use of specific solder alloys may help mitigate voiding.
3. Use a solder paste that works well with the surface finish to minimize voiding.
4. Use “low voiding” solder pastes to reduce the overall potential for voiding.
5. Optimize the stencil design for the components to allow for complete wetting and gas escape routes.

FUTURE WORK

Voiding is an issue for via in pad circuit board designs, regardless of the solder paste used. Via plugging options and stencil designs can help to mitigate this type of voiding. Work is planned on via in pad voiding issues and will be presented at a future technical conference.

ACKNOWLEDGEMENTS

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